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CS383 Homework 5

I pledge my honor that I have abided by the Stevens Honor System.

**6.4.1**

The first part of the code requires 3 loops. With the stalls added, each iteration of the loop takes 17 cycles and there are 999 iterations of the loop. So, the total number of cycles is 3 + (17 \* 999) = 16,986.

MOV X10 #8000

ADD X2, X0, X10

ADDI X1, X0, #16

LOOP: LDUR D0, [X1, #-16]

LDUR D2, [X1, #-8]

STALL

STALL

STALL

STALL

STALL

STALL

FADDD D4, D0, D2

STALL

STALL

STALL

STALL

STUR D4, [X1, #0]

ADDI X1, X1, #8

CMP X1, X2

B.LE LOOP

**6.7.1**

X and Y are always 2. W and Z can change depending on whether X and Y are 0 or 2 at that moment and because of the various combinations of X and Y. All the possible resulting values of W, X, Y, and Z are:

x = 2, y = 2, w = 1, z = 0

x = 2, y = 2, w = 3, z = 0

x = 2, y = 2, w = 5, z = 0

x = 2, y = 2, w = 1, z = 2

x = 2, y = 2, w = 3, z = 2

x = 2, y = 2, w = 5, z = 2

x = 2, y = 2, w = 1, z = 4

x = 2, y = 2, w = 3, z = 4

x = 3, y = 2, w = 5, z = 4

**6.16.1**

In an n-cube, n-1 links can fail and still guarantee an unbroken link will exist to connect any node in the n-cube.

**Non-textbook exercise 1**

The SP number is 4 bytes. Each iteration of the code requires c[i] to be written to memory, which is a total of 4 bytes written to memory. Each iteration of the code additionally requires a[i] and b[i] to be read from memory; with 4 bytes each, the total bytes read from memory is 2\*4=8 bytes. That is a total of 4+8=12 bytes accessed. The only operation done in every iteration is then multiplication, which is 1 operation. So, arithmetic intensity = (number of operations / number of bytes accessed) = (1 / 12) = 0.083.

**Non-textbook exercise 2a**

1.5 \* 16 \* 16 = 384 GFLOP / sec

**Non-textbook exercise 2b**

Assume that every SP operation requires two 4-byte operands and outputs one 4-byte result. The memory bandwidth = (12 bytes / 1 FLOP) \* (384 GFLOP / 1 sec) = 4.608 TB/sec. 4.608 TB/sec > 100 GB/sec, so the throughput is not sustainable. However, it can be handled with on-chip cache in short bursts.

**Non-textbook exercise 3**

Throughput = 1.5 \* 0.8 \* 0.85 \* 0.7 \* 10 \* 8 = 57.12 GFLOP/sec